Managed by Fermi Research Alliance, LLC for the U.S. Department of Energy Office of Science

Notes on DDCP and OEI

Ryan A. Rivera
Scientific Computing Division
Frameworks, DAQ, and Electronics department
16 April, 2020

Overview

- Compare DDCP and OEI (*otsdaq* Ethernet Interface)
  - Identify potential conflicts and open questions.
- Propose design approach to Ethernet piece of the uTCA FPGA digitizer demo.
- Propose an approach to resolving IP addresses or setting IP addresses in the field.
  - Favor protocol-based solutions.
    - Avoid DIP switch or other hardware-based solution that may preclude use of other commercial boards.

Notes on DDCP vs OEI (1 of 2)

- In DDCP, “Server” is the hardware, “Client” is requesting software
- Max size in DDCP is 9000 bytes. OEI follows the 1500 byte Ethernet MTU standard, which leaves 1472 bytes for UDP payload.
  - The OEI protocol allows for up to 182 quadwords (quadwords = 8-bytes).
- DDCP is expecting hardware to send from port 65000.
  - OEI sends from port 2001.
- All DDCP messages use special protocol header (6*16 + 1*32 + 3*64 ⇒ 20 bytes). Has extra notion of “slot” and “feature” .. “index” is like address.
  - OEI protocol is 10 byte header.

Notes on DDCP vs OEI (2 of 2)

- DDCP Expects a tunable delay on the FPGA transmit side between packets to throttle.
  - Currently not in OEI
- DDCP allows unsolicitied requests from hardware (i.e. bidirectional reads), not how OEI works right now.
- DDCP does not currently define how to set IP address of hardware or destination addresses.
- DDCP does not currently define if hardware must be pingable, or how ARP handling should work.

Approach from OEI to DDCP

- *otsdaq* provides full rate UDP firmware solution (essentially DDCP) based on generic RTL:
  - In use since 2010 at test beam.
  - Documented on Redmine:
    - https://cdcvs.fnal.gov/redmine/projects/otsdaq/wiki/OtS_Ethernet_Interface
  - Also, the full otsdaq project is found here, led by SCD/FDE: otsdaq.fnal.gov

- Two primary blocks:
  - Ethernet controller
  - OEI protocol wrapper
    - This block will likely need to be replaced with the new “DDCP protocol wrapper”

Features of Ethernet Controller

- Repo location:
  - https://cdcvs.fnal.gov/redmine/projects/otsdaq/repository/firmware/revisions/develop/entry/cactus/components/ots_ethernet/firmware/dev/ActiveHDL_proj/ethernet_controller/compile/ethernet_controller.vhd
- Implemented in pure vhdl/Verilog with no memory or vendor IP elements.
- Inputs: full self MAC, IP, and PORT
- Handles ARP replies and broadcasts
- Will reply to any ARP
  - fail-safe useful in determining current MAC/IP of hardware
- Handles ICMP ping replies
- Ignores anything that is not ARP, addressed UDP, or addressed ICMP.
- Single-byte special packet handling:
  - Change IP (disabled now due to risk, but could enable),.. Functionality moved to OEI protocol wrapper so the packet formation was more complex
  - 0 → get version
  - 1 → special strobe 1 synced with client address capture
  - 2 → special strobe 2 synced with client address capture
  - 3-FF → no-op (to keep software OS sockets alive)

Features of OEI Protocol Wrapper

- After reset, low 8-bits of address default to user specified value (i.e. can be hardcoded in firmware project or come from pins).
  - OEI Port is always hardcoded to 2001.
- OEI segments 64-bit address space into “internal” and “external” user space
  - For example, OEI full MAC and IP can be changed by writing to the internal address space: https://otsdaq.fnal.gov/docs/oei_address_space.html
- OEI has two transmit channels, “burst” (FPGA pushes data to software without requests) and “control” (software pulls data from FPGA).
  - With separate destination addresses
  - “Control” also has reply-to-sender operation

Proposed Approach

- Throw out OEI protocol wrapper, keep Ethernet controller
- Create new DDCP wrapper
  - DDCP wrapper implements the 20-byte header handling
  - Map DDCP “_feature” to essentially the “internal address space” OEI concept, for example, to change FPGA MAC address and IP address,.
  - Map DDCP “_index” to OEI “external address space” address

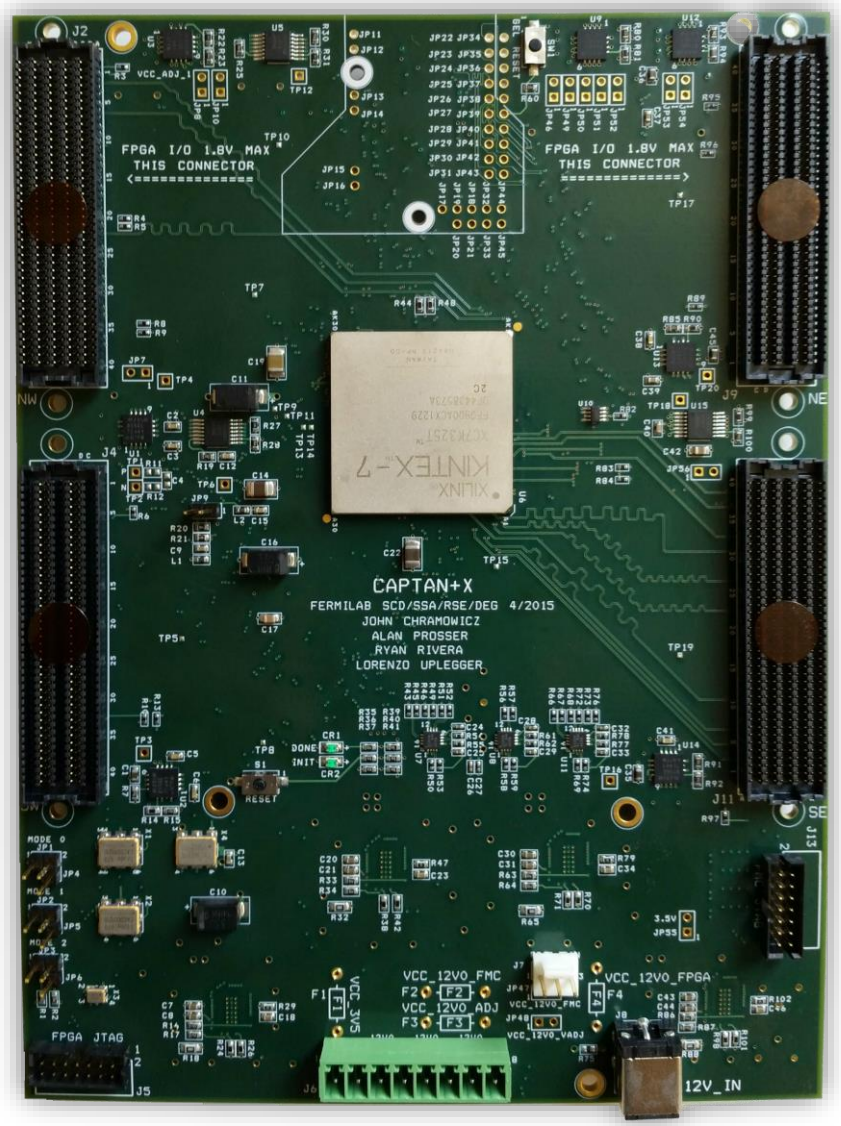
Open Questions

- What kind of activity is on the IPMI/backplane network?
  - Is it quiet? If so, consider single-byte IP.
  - Other special expected behavior on this network?
- Do we want FPGA responses to always go to one place (as defined by request source)? Or will data potentially go to a different sink than requester?
- Do we want FPGA to generate unsolicited requests? If so, which client is targeted?
- Should there be an protocol operation to indicate index increments for count versus does NOT increment for count?
  - For example, reading from target FIFO.
    - Have found this useful in OEI user space.

Backup

SCD/FDE Applicable Project Experience (4 of 8)

- Designed and supported FPGA card by SCD/FDE
- CAPTAN+ (“CAPTAN plus”) is the next generation CAPTAN card.
  - A leap from Xilinx 4 series to 7 series.
  - The ‘X’ stands for “eXtreme” for its support of 10G links.
- **Features:**
  - Gigabit Ethernet
  - 4 FMC connectors, 16 Links
    - 2 HPC, 2 LPC
    - High-speed Links per FMC:
      - SE=10, NW=4, NE=1, SW=1.
  - 400 GPIO
  - 12V Input Power Block



SCD/FDE Applicable Project Experience (5 of 8)

- Completed a test beam project at Fermilab in 2016
  - Real-time event assembly conducted in µTCA form factor.